

DATA SHEET

74LVT640

**3.3V Octal transceiver with direction pin;
inverting (3-State)**

Product specification
Supersedes data of 1996 Oct 01
IC23 Data Handbook

1998 Feb 19

3.3V Octal transceiver with direction pin; inverting (3-State)

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FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT640 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable (\overline{OE}) input for easy cascading and a Direction (DIR) input for direction control.

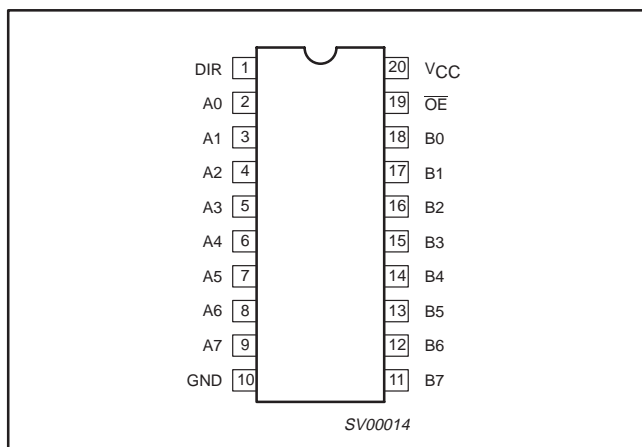
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF};$ $V_{CC} = 3.3\text{V}$	2.3 2.4	ns
C_{IN}	Input capacitance DIR, \overline{OE}	$V_I = 0\text{V}$ or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0\text{V}$ or 3.0V	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{V}$	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	-40°C to $+85^{\circ}\text{C}$	74LVT640 D	74LVT640 D	SOT163-1
20-Pin Plastic SSOP	-40°C to $+85^{\circ}\text{C}$	74LVT640 DB	74LVT640 DB	SOT339-1
20-Pin Plastic TSSOP	-40°C to $+85^{\circ}\text{C}$	74LVT640 PW	74LVT640PW DH	SOT360-1

PIN CONFIGURATION



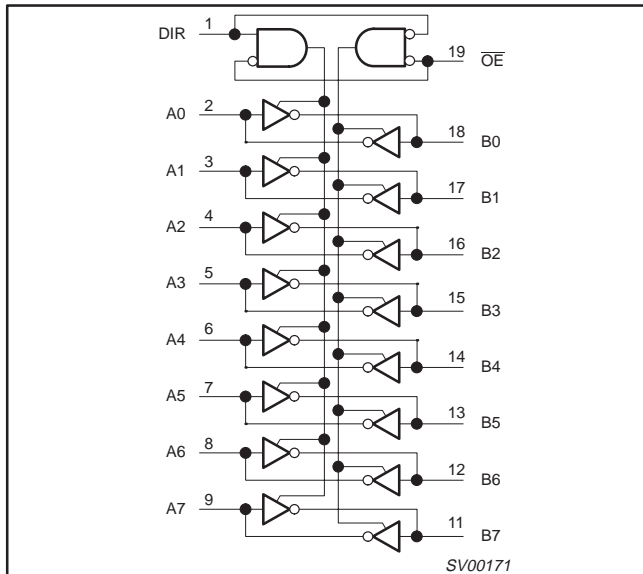
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	\overline{OE}	Output enable input (active–Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

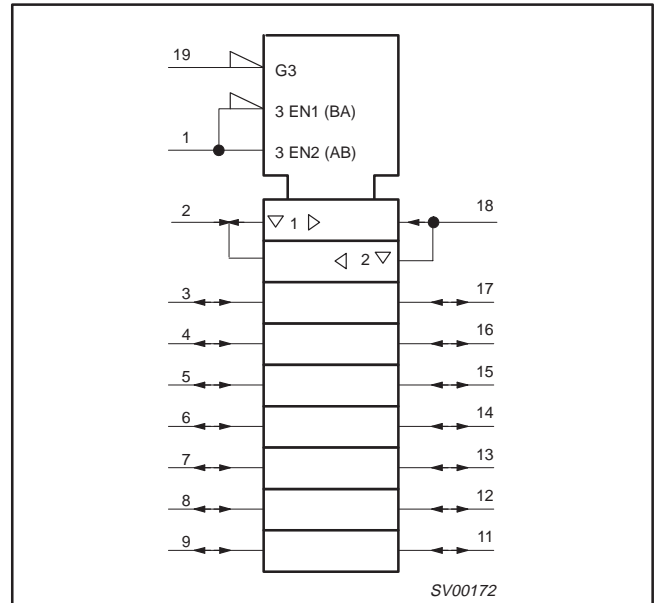
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{OEn}	DIR	A_n	B_n
L	L	$\overline{B_n}$	Inputs
L	H	Inputs	$\overline{A_n}$
H	X	Z	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "Off" state

ABSOLUTE MAXIMUM RATINGS^{1,2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1$ kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	$^{\circ}\text{C}$

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to $+85^{\circ}\text{C}$			
			MIN	TYP ¹	MAX	
V_{IK}	Input clamp voltage	$V_{CC} = 2.7\text{V}; I_{IK} = -18\text{mA}$		-0.9	-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = 2.7$ to $3.6\text{V}; I_{OH} = -100\mu\text{A}$	$V_{CC}-0.2$	$V_{CC}-0.1$		V
		$V_{CC} = 2.7\text{V}; I_{OH} = -8\text{mA}$	2.4	2.5		
		$V_{CC} = 3.0\text{V}; I_{OH} = -32\text{mA}$	2.0	2.2		
V_{OL}	Low-level output voltage	$V_{CC} = 2.7\text{V}; I_{OL} = 100\mu\text{A}$		0.1	0.2	V
		$V_{CC} = 2.7\text{V}; I_{OL} = 24\text{mA}$		0.3	0.5	
		$V_{CC} = 3.0\text{V}; I_{OL} = 16\text{mA}$		0.25	0.4	
		$V_{CC} = 3.0\text{V}; I_{OL} = 32\text{mA}$		0.3	0.5	
		$V_{CC} = 3.0\text{V}; I_{OL} = 64\text{mA}$		0.4	0.55	
I_I	Input leakage current	$V_{CC} = 0$ or $3.6\text{V}; V_I = 5.5\text{V}$	Control pins	1	10	μA
		$V_{CC} = 3.6\text{V}; V_I = V_{CC}$ or GND		± 0.1	± 1	
		$V_{CC} = 3.6\text{V}; V_I = 5.5\text{V}$	I/O Data pins ⁴	1	20	
		$V_{CC} = 3.6\text{V}; V_I = V_{CC}$		0.1	1	
		$V_{CC} = 3.6\text{V}; V_I = 0$		-1	-5	
I_{OFF}	Output off current	$V_{CC} = 0\text{V}; V_I$ or $V_O = 0$ to 4.5V		1	± 100	μA
I_{HOLD}	Bus Hold current A inputs ^{NO TAG}	$V_{CC} = 3\text{V}; V_I = 0.8\text{V}$	75	150		μA
		$V_{CC} = 3\text{V}; V_I = 2.0\text{V}$	-75	-150		
		$V_{CC} = 0\text{V}$ to $3.6\text{V}; V_{CC} = 3.6\text{V}$	± 500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	$V_O = 5.5\text{V}; V_{CC} = 3.0\text{V}$		60	125	μA
$I_{PU/PD}$	Power up/down 3-State output current ³	$V_{CC} \leq 1.2\text{V}; V_O = 0.5\text{V}$ to $V_{CC}; V_I = \text{GND}$ or $V_{CC}; \text{OE/OE} = \text{Don't care}$		15	± 100	μA
I_{CCH}	Quiescent supply current	$V_{CC} = 3.6\text{V};$ Outputs High, $V_I = \text{GND}$ or $V_{CC}, I_O = 0$		0.13	0.19	mA
I_{CCL}		$V_{CC} = 3.6\text{V};$ Outputs Low, $V_I = \text{GND}$ or $V_{CC}, I_O = 0$		3	12	
I_{CCZ}		$V_{CC} = 3.6\text{V};$ Outputs Disabled; $V_I = \text{GND}$ or $V_{CC}, I_O = 0$		0.13	0.19	
ΔI_{CC}	Additional supply current per input pin ²	$V_{CC} = 3\text{V}$ to $3.6\text{V};$ One input at $V_{CC}-0.6\text{V},$ Other inputs at V_{CC} or GND		0.1	0.2	mA

NOTES:

- All typical values are at $V_{CC} = 3.3\text{V}$ and $T_{amb} = 25^{\circ}\text{C}$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec . From $V_{CC} = 1.2\text{V}$ to $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ a transition time of $100\mu\text{sec}$ is permitted. This parameter is valid for $T_{amb} = +25^{\circ}\text{C}$ only.
- Unused pins at V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

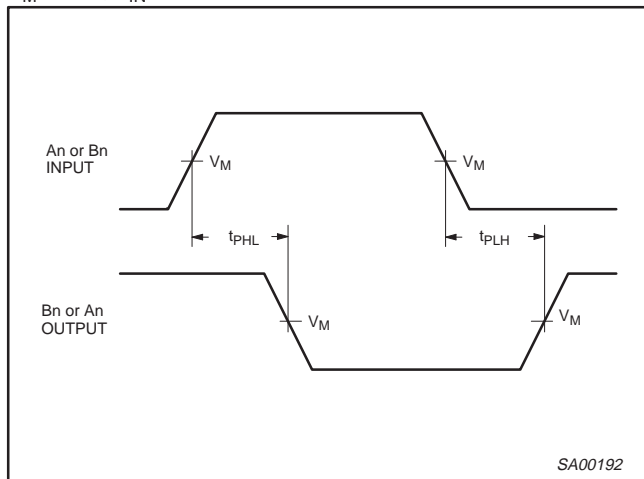
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V + 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP ¹	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	NO TAG	1.0 1.0	2.3 2.4	3.7 3.3	4.5 3.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	NO TAG	1.1 1.5	3.5 3.6	5.3 5.3	6.9 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	NO TAG	2.2 2.0	3.7 3.1	5.0 4.5	5.6 4.5	ns

NOTES:

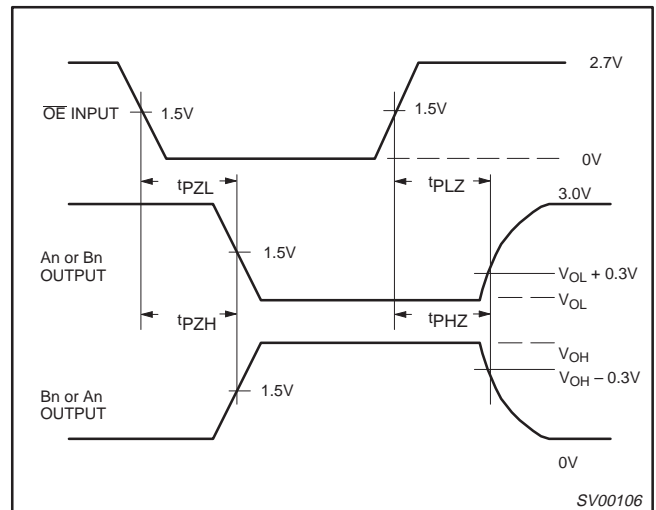
- All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

AC WAVEFORMS

$V_M = 1.5V$, $V_{IN} = \text{GND to } 2.7V$



Waveform 1. Input (An or Bn) to Output (Bn or An) Propagation Delays

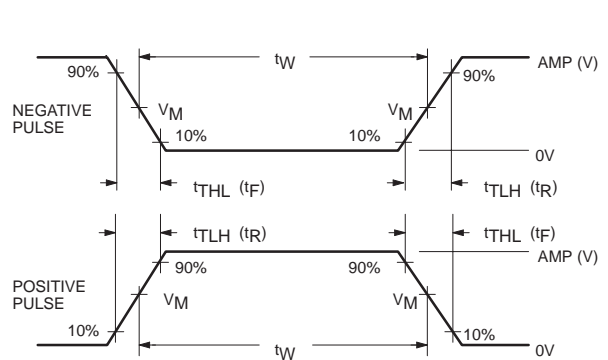
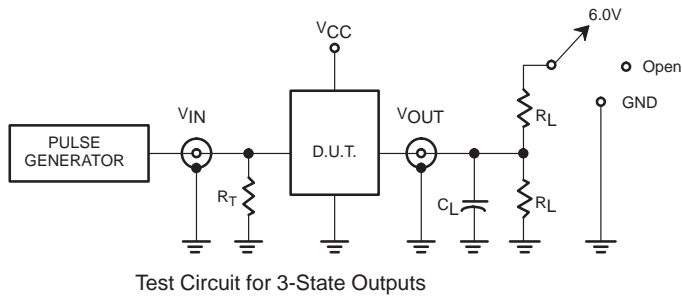


Waveform 2. 3-State Output Enable and Disable Times

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TEST CIRCUIT AND WAVEFORMS



SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

SV00092

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

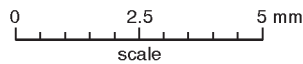
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

3.3V Octal transceiver with direction pin; inverting (3-State)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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